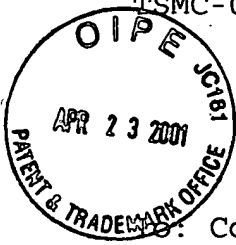


TSMC-00-338



April 12, 2001

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Commissioner of Patents and Trademarks
Washington, D.C. 20231

Fr: George O. Saile, Reg. No. 19,572
20 McIntosh Drive
Poughkeepsie, N.Y. 12603

Subject:

Serial No. 09/785,114 02/20/01

Pin-Shyne Chin, Wen-Tye Yue,
Hsien-Chin Peng

A LOW LEAKAGE ONE TRANSISTOR STATIC
RANDOM ACCESS MEMORY

Grp. Art Unit: 2812

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation
In An Application.

The following Patents and/or Publications are submitted to
comply with the duty of disclosure under CFR 1.97-1.99 and
37 CFR 1.56. Copies of each document is included herewith.

U.S. Patent 6,078,087 to Huang et al., "SRAM Memory Device
with Improved Performance", discloses a TFT SRAM layout.

U.S. Patent 5,686,336 to Lee, "Method of Manufacture of
Four Transistor SRAM Cell Layout", discloses a 4T SRAM layout.

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U.S. Patent 5,953,606 to Huang et al., "Method for Manufacturing a TFT SRAM Memory Device with Improved Performance", discloses a TFT SRAM layout.

Sincerely,

A handwritten signature in black ink, appearing to read 'SBA', with a long horizontal line extending to the right.

Stephen B. Ackerman,
Reg. No. 37761